SPECIFICATION AMENDMENTS

Please amend that portion of the specification appearing from line 27 on page 32 to line 17 on page 40 as follows:

(2) A multilayer electronic substrate as ~~claimed~~ described in (1) wherein:

said portion of the first conductor layer, which corresponds to the trimming portion of said resistor, is formed by a mask pattern printing operation when said first conductor layer is printed.

(3) A multilayer electronic substrate as ~~claimed~~ described in ~~claim~~ (1) wherein:

the portion of said first conductor layer, which corresponds to the trimming portion of said resistor, is formed by a trimming operation after said first conductor layer has been printed in a solid manner.

(4) A multilayer electronic substrate as ~~claimed~~ described in ~~claim~~ (1), (2) or (3) wherein:

said insulating region is formed in an integral body with the insulator arranged between said first conductor layer and said second conductor layer.

(5) A multilayer electronic substrate as ~~claimed~~ described in ~~claim~~ (1), (2) or (3) wherein:

said insulating region is separately formed with reference to the insulator arranged between said first conductor layer and said second conductor layer, and is inserted to be arranged.

(6) A multilayer electronic substrate as ~~claimed~~ described in ~~claim~~ (1), (2), (3), (4) or (5) wherein:

a circuit pattern protection layer is provided in such a manner that said circuit pattern protection layer covers said insulator, said second conductor layer, and said resistor.

(7) An electronic appliance containing:

a multilayer electronic substrate as a structural component, which is manufactured by comprising:

a first conductor layer arranged by providing an insulating region on an insulating substrate;

an insulator arranged by embedding said insulating region on said first conductor layer; and

a resistor arranged on said insulator, and a second conductor layer for sandwiching said resistor to be connected to said resistor; and in which

said resistor is trimmed so as to adjust an electric characteristic of a circuit.

(8) An electronic appliance as ~~claimed~~ described in ~~claim~~ (7) wherein:

said electronic appliance containing said multilayer electronic substrate as the structural component corresponds to a heat wire type airflow meter for measuring a flow rate of air by controlling a current flowing through a heat wire.

(9) A method of manufacturing a multilayer electronic substrate, comprising:

a first step for arranging a first conductor layer on an insulating substrate;

a second step for forming a gap in said first conductor layer;

a third step for arranging an insulator on said

first conductor layer and in said gap;

a fourth step for arranging a resistor on said insulator, and a second conductor layer which sandwiches said resistor and is connected to said resistor; and

a fifth step for trimming said resistor so as to adjust an electric characteristic of a circuit and to form a trimming portion.

(10) A manufacturing method of a multilayer electronic substrate as ~~claimed~~ described in ~~claim~~ (9) wherein:

the gap of said second step is formed by a mask pattern printing operation when said first conductor layer is printed in said first step.

(11). A manufacturing method of a multilayer electronic substrate as ~~claimed~~ described in ~~claim~~ (9) wherein:

the gap of said second step is formed by a trimming operation after said first conductor layer has been printed in a solid manner in said first step.

(12) A manufacturing method of a multilayer electronic substrate as ~~claimed~~ described in ~~claim~~ (9), (10) or (11) wherein:

after said fifth step for trimming said resistor so as to adjust the electric characteristic of the circuit and to form the trimming portion,

a sixth step is provided in which a circuit pattern protection layer is arranged on said first insulator, said resistor, and said second conductor layer.

(13) A multilayer electronic substrate manufactured by comprising: a first conductor layer arranged on an insulating substrate; a first insulator arranged on said first conductor

layer; a first resistor arranged on said first insulator; a second conductor layer for sandwiching said first resistor to be connected to said first resistor;

a second insulator arranged on said first insulator, said first resistor, and said second conductor;

a second resistor arranged on said second insulator, and a third conductor for sandwiching said second resistor to be connected to said second resistor; and

a circuit pattern protection layer arranged on said second insulator, said third conductor, and said second resistor; wherein:

said first resistor is trimmed so as to adjust an electric characteristic of a circuit and said second resistor is trimmed so as to adjust an electric characteristic of a circuit;

a portion of said first conductor layer, which corresponds to a first trimming portion of said first resistor, is constituted by a first insulating region; and a portion of said first conductor layer, which corresponds to a second trimming portion of said second resistor, is constituted by a second insulating region.

(14) A multilayer electronic substrate as ~~claimed~~ described in ~~claim~~ (13) wherein:

both the portion of said first conductor layer, which corresponds to the first trimming portion of said first resistor, and the portion of said second conductor layer, which corresponds to the second trimming portion of said second resistor 18, are formed by a mask pattern printing operation when said first conductor layer is printed.

(15) A multilayer electronic substrate as ~~claimed~~ described in ~~claim~~ (13) wherein:

both the portion of said first conductor layer, which corresponds to the first trimming portion of said first resistor, and the portion of said second conductor layer, which corresponds to the second trimming portion of said second resistor, are formed by a trimming operation after said first conductor layer has been printed in a solid printing manner.

(16) A multilayer electronic substrate as ~~claimed~~ described in ~~claim~~ (13), (14) or (5) wherein:

both said first insulating region and said second insulating region are formed in an integral body with the insulator arranged between said first conductor layer and said second conductor layer.

(17) A multilayer electronic substrate as ~~claimed~~ described in ~~claim~~ (13), (14) or (15) wherein:

both said first insulating region and said second insulating region are separately formed with reference to the insulator arranged between said first conductor layer and said second conductor layer.

(18) An electronic appliance containing:

a multilayer electronic substrate as a structural component, which is manufactured by comprising:

a first conductor layer arranged on an insulating substrate; a first insulator arranged on said first conductor layer; a first resistor arranged on said first insulator; a second conductor layer for sandwiching said first resistor to be connected to said first resistor;

a second insulator arranged on said first insulator, said first resistor, and said second conductor;

a second resistor arranged on said second insulator, and a third conductor for sandwiching said second resistor to be connected to said second resistor; and

a circuit pattern protection layer arranged on said second insulator, said third conductor, and said second resistor; wherein:

said first resistor is trimmed so as to adjust an electric characteristic of a circuit and said second resistor is trimmed so as to adjust an electric characteristic of a circuit; and

both said first resistor and said second resistor are trimmed in order to adjust an electric characteristic of a circuit.

(19) An electronic appliance as ~~claimed~~ described in ~~claim~~ (18) wherein:

said electronic appliance containing said multilayer electronic substrate as the structural component corresponds to a heat wire type airflow meter for measuring a flow rate of air by controlling a current which flows though a heat wire.

(20) A method of manufacturing a multilayer electronic substrate, comprising:

a first step for arranging a first conductor layer on an insulating substrate;

a second step for forming a first gap and a second gap in the first conductor layer;

a third step for arranging a first insulator on the first conductor layer and in the first gap and the second gap;

a fourth step for arranging a first resistor on the first insulator, and a second conductor layer which sandwiches the first resistor and is connected to the first resistor;

a fifth step for trimming the first resistor so as to adjust an electric characteristic of a circuit and to form a trimming portion;

a sixth step for arranging a second insulator on the second conductor layer,

a seventh step for arranging second resistor on the second insulator, and a third conductor which sandwiches the second resistor and is connected to the second resistor; and

an eighth step for trimming the second resistor so as to adjust an electric characteristic of a circuit and to form a trimming portion.

(21) A method of manufacturing a multilayer electronic substrate as ~~claimed~~ described in ~~claim~~ (20),

wherein the second step is executed by a mask pattern printing operation when the first conductor layer is printed in the first step.

(22) A method of manufacturing a multilayer electronic substrate as ~~claimed~~ described in ~~claim~~ (20),

wherein the second step is executed by a trimming operation after the first conductor layer has been printed in a solid step in the first step.

(23) A method of manufacturing a multilayer electronic substrate as ~~claimed~~ described in ~~claim~~ (20), (21) or (22),